Torc: Towards an Open-Source Tool Flow

Neil Steiner,[1] Aaron Wood,[1] Hamid Shojaei,[1,2] Jacob Couch,[3] Peter Athanas,[3] and Matthew French[1]

[1] Information Sciences Institute
neil.steiner@isi.edu, awood@isi.edu, mfrench@isi.edu

[2] University of Wisconsin-Madison
hshojaei@wisc.edu

[3] Virginia Tech
jacouch@vt.edu, athanas@vt.edu

What is Torc?

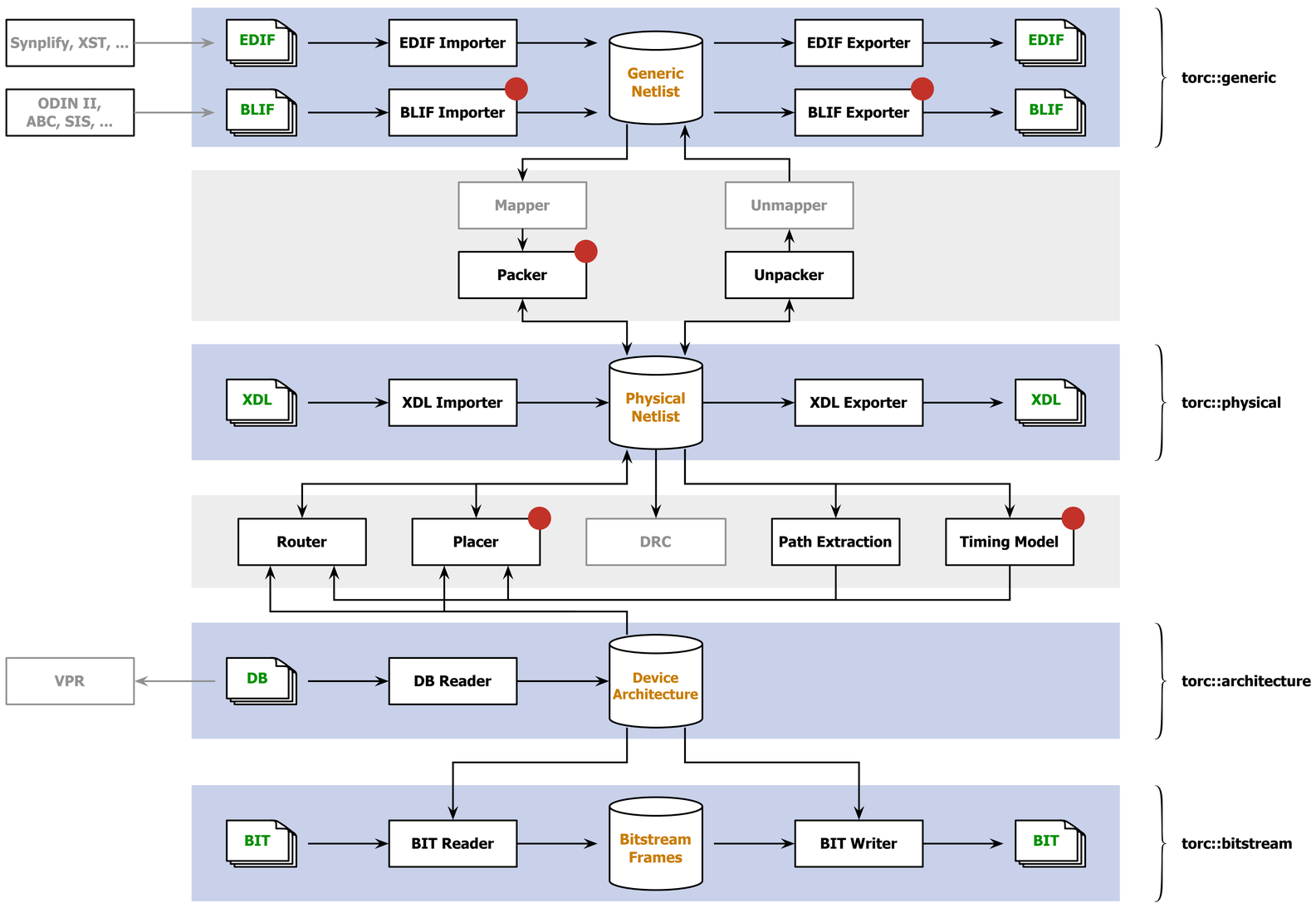
- A C++ open-source project
- Collection of APIs and CAD tools
- Released under GNU GPL license
- Hosted on SourceForge
- Free of proprietary code or data

Motivation

- Needed a robust circuit manipulation environment
- Too many researchers rewrite their own tools
- Facilitate EDA/CAD research with real device data
- Share some of the collectively acquired knowledge

Uses and Applications

- CAD tool research
- Device architecture exploration
- Hardware autonomy research
- Partial runtime reconfiguration
- Low-power CAD
- Radiation effect mitigation
- Security/anti-tamper
- Health monitoring



Generic API:

- Works with unmapped netlists
- Reads, modifies, writes EDIF

Physical API:

- Works with mapped netlists
- Reads, modifies, writes XDL

Architecture API:

- Device wiring, logic, and package data
- Complete support for largest devices
- Built from non-proprietary XDLRC

Bitstream API:

- Read, modify, write Xilinx bitstreams
- No understanding of frame *contents*

Router:

- PathFinder implementation

Unpacker:

- Splits slices into constituent components
- Facilitates natural design manipulation

Supported Families (139 Devices):

Virtex, VirtexE, Virtex2, Virtex2P, Virtex4, Virtex5, Virtex6, Virtex6L, Spartan3E, Spartan6, Spartan6L

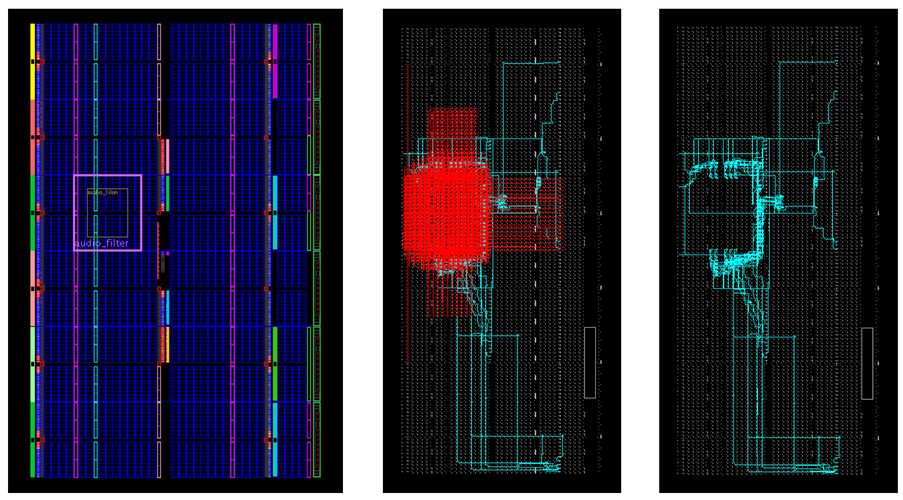
http://torc.isi.edu

Design Goals:

- Designed for ten year shelf life
- Designed for completeness
- Optimized for very large devices
- Optimized for very large designs
- Designed for embedding
- Designed for testability
- Designed for conditional compilation
- Designed for simplicity
- Intended for researchers

Ongoing and Planned Work:

- Rehost unpacker on latest code
- Develop/integrate packer, placer, BLIF import/export, timing models
- Complete all unit tests
- Complete Doxygen documentation
- Characterize performance
- Add constraint support
- Add TCL scripting
- Complete bitstream frame index mapping
- Designed for simplicity
- Intended for researchers



OpenPR. Third party tool. Uses Torc to rigorously prohibit ISE router from using reserved resources. Floorplan on left shows static and dynamic areas. "Blocker" route in center prevents any wiring from passing through dynamic region. Resulting static design on right.

Information Sciences Institute

WISCONSIN
UNIVERSITY OF WISCONSIN–MADISON

Virginia Tech

USC